CLAIMS

1. An apparatus for performing a boundary scan test, comprising:

an asynchronous flip-flop having a data input, a data output, a system clock input, a set input, and a reset input; and

a test controller having a test clock input, a first test data output, and a second test data output, the first test data output being connected to the set input of the asynchronous flip-flop, the second test data output being connected to the reset input of the asynchronous flip-flop, the test controller being configured to control the asynchronous flip-flop through the set input and the reset input.

2. An apparatus for performing a boundary scan test as recited in claim 1, wherein the test controller is configured to communicate with the asynchronous flip-flop without communicating through intervening multiplexing circuitry.

3. An apparatus for performing a boundary scan test as recited in claim 1, wherein the test controller is configured to communicate directly with the asynchronous flip-flop.

4. An apparatus for performing a boundary scan test as recited in claim 1, wherein the first test data output of the test controller is capable of asserting the set input of the asynchronous flip-flop, asserting the set input causing a high signal to be maintained by the asynchronous flip-flop.

5. An apparatus for performing a boundary scan test as recited in claim 1, wherein the second test data output of the test controller is capable of asserting the reset input of the asynchronous flip-flop, asserting the reset input causing a low signal to be maintained by the asynchronous flip-flop.

6. An apparatus for performing a boundary scan test as recited in claim 1, wherein the set input is configured to dominate the reset input such that simultaneously asserting both the set input and the reset input causes a high signal to be maintained by the asynchronous flip-flop.

7. An apparatus for performing a boundary scan test as recited in claim 1, wherein the reset input is configured to dominate the set input such that simultaneously asserting both the set input and the reset input causes a low signal to be maintained by the asynchronous flip-flop.

8. An apparatus for performing a boundary scan test as recited in claim 1, wherein the asynchronous flip-flop is configured to transmit a signal received at the data input to the data output in accordance with the system clock input when both the set input and the reset input are not asserted.

9. An apparatus for performing a boundary scan test as recited in claim 1, wherein the test controller is a test access port (TAP) controller compliant with an IEEE 1149.1 standard.

10. An apparatus for performing a boundary scan test as recited in claim 9, wherein the first test data output is a test data in (TDI) pin of the TAP controller.

11. An apparatus for performing a boundary scan test as recited in claim 9, wherein the second test data output is a test reset (TRST) pin of the TAP controller.

12. An apparatus for performing a boundary scan test, comprising:

an asynchronous flip-flop having a data input, a data output, a system clock input, a set input, and a reset input; and

a test controller having a test clock input, a first test data output, and a second test data output, the first test data output being connected to the set input of the asynchronous flip-flop, the second test data output being connected to the reset input of the asynchronous flip-flop, the test controller being configured to communicate with the asynchronous flip-flop without communicating through intervening multiplexing circuitry.

13. An apparatus for performing a boundary scan test as recited in claim 12, wherein the first test data output of the test controller is capable of asserting the set input of the asynchronous flip-flop and the second test data output of the test controller is capable of asserting the reset input of the asynchronous flip-flop, asserting the set input causing a high signal to be maintained by the asynchronous flip-flop and asserting the reset input causing a low signal to be maintained by the asynchronous flip-flop.

14. An apparatus for performing a boundary scan test as recited in claim 12, wherein the asynchronous flip-flop is configured to transmit a signal received at the data input to the data output in accordance with the system clock input when both the set input and the reset input are not asserted.

15. A method for integrating a boundary scan cell into a circuit, comprising:

connecting a data output port of an asynchronous flip-flop to a pin of a boundary scan compatible device;

connecting a first output port of a test controller to a set input port of the asynchronous flip-flop; and

connecting a second output port of the test controller to a reset input port of the asynchronous flip-flop,

wherein the first output port and the second output port of the test controller are connected to the asynchronous flip-flop without connecting to multiplexing circuitry intervening between the test controller and the asynchronous flip-flop.

16. A method for integrating a boundary scan cell into a circuit as recited in claim 15, further comprising:

interposing a driver between the data output port and the pin, the data output port being connected to an input of the driver and the pin being connected to an output of the driver.

17. A method for integrating a boundary scan cell into a circuit as recited in claim 15, further comprising:

connecting a system clock circuit to a system clock input of the asynchronous flip-flop; and

connecting a test clock circuit to a test clock input of the test controller.

18. A method for operating a boundary scan cell, comprising:

communicating a first signal and a second signal from a test controller to an asynchronous flip-flop in accordance with a boundary scan timing signal, wherein the communicating is performed without having to communicate through a multiplexing circuit;

receiving the first signal at a set input of the asynchronous flip-flop; and

receiving the second signal at a reset input of the asynchronous flip-flop,

wherein a high state of the first signal causes the asynchronous flip-flop to maintain a high state, a high state of the second signal causes the asynchronous flip-flop to maintain a low

state, and a low state of both the first signal and the second signal causes the asynchronous flip-flop to operate in a normal function mode.

19. A method for operating a boundary scan cell as recited in claim 18, wherein a high state of at least one of the first signal and the second signal causes the asynchronous flip-flop to operate in a boundary scan test mode.

20. A method for operating a boundary scan cell as recited in claim 18, wherein a state maintained by the asynchronous flip-flop in response to the high state of at least one of the first signal and the second signal represents a portion of a boundary scan test input.

21. A method for operating a boundary scan cell as recited in claim 18, wherein simultaneously receiving both the first signal and the second signal in a high state causes the asynchronous flip-flop to maintain a high state.

22. A method for operating a boundary scan cell as recited in claim 18, wherein simultaneously receiving both the first signal and the second signal in a high state causes the asynchronous flip-flop to maintain a low state.

23. A method for operating a boundary scan cell as recited in claim 18, further comprising:

activating the asynchronous flip-flop to allow a state maintained by the asynchronous flip-flop to be transmitted through a data output of the asynchronous flip-flop to a pin of a boundary scan compatible device.

24. A method for operating a boundary scan cell as recited in claim 18, wherein the normal function mode includes transmission of a signal received at a data input of the asynchronous flip-flop to a data output of the asynchronous flip-flop in accordance with a system clock signal received at a clock input of the asynchronous flip-flop.